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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,970	02/05/2004	Charles A. Miller	P199-US	5200

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EXAMINER	
CHAN, EMILY Y	

ART UNIT	PAPER NUMBER
2829	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/772,970	MILLER, CHARLES A.	
	Examiner	Art Unit	
	Emily Y. Chan	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-30 and 36-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-30,39,44 and 46-49* is/are rejected.

7)☒ Claim(s) *36-38,40-43 and 45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 44 is objected to because of the following informalities: claim 44 duplicates the claim 39. Therefore, the examiner assumes that the claim 44 is dependent on claim 27. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 16-30 and 46-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slupsky (US Patent 6,885,202) in view of Rostoker (US Patent No. 5,838,163).

With respect to claims 16 and 27, Slupsky ('202) discloses a semiconductor wafer (see Fig. 2, 30) comprising:

a plurality of dies (12) each comprising functional circuitry (see Col. 2, line 47 " to test electronic circuits 12 on wafer 30"); and

electrically conductive structures (wireless I/O cells 14) configured to contactlessly receive test signals (see Col. 2, lines 4-5) for testing the functional circuitry (see Col. 2, lines 52-54).

Slupsky ('202) does not disclose an electrically conductive shielding plane disposed between the conductive structures and the functional circuitry.

Rostoker ('163) discloses a semiconductor wafer (see Fig.1, 104) comprising a plurality of dies (102a,102b, 102c and 102d), each comprising functional circuitry (pads 220) (see Col. 10, lines 17-18 "using the same limited number of pads for both burning-in and for cross-check testing") and electrically conductive structures (see Col. 6, lines 15-24). Rostoker ('163) exclusively discloses an electrically conductive shielding plane (the overlying grid of lines) provided for electromagnetic (EM) shielding of the device (dies) on the wafer (see Col. 6, lines 6-8). The examiner notes that Rostoker ('163) discloses the shielding line instead of shielding plane; however, it would have been obvious to one of ordinary skill in the art to have changed the shielding line into shielding plane as desired (see MPEP 2144.04 IV " CHANGE IN SIZE, SHAPE").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate Rostoker ('163) 's overlying grid of lines as an electrical conductive shielding plane into Slupsky ('202)'s semiconductor wafer so that Slupsky ('202)'s wafer comprises an electrically conductive shielding plane as claimed because Rostoker ('163) discloses that his overlying grid of lines provides electromagnetic (EM) shielding of the device (dies) on the wafer (see Col. 6, lines 6-8).

With respect to claim 17, Slupsky ('202) discloses that each die (12) comprises a set of said conductive structures (wireless I/O cells 14).

With respect to claim 18, Slupsky ('202) discloses each of said conductive structures (wireless I/O cells 14) in a set of said conductive structures are electrically connected to a plurality of said dies (12) (see Fig. 2).

With respect to claim 19, Slupsky ('202) discloses that the conductive structures are electromagnetically (see Col. 2, line 34, " a magnetic interface for sending and receiving signals") coupleable to a tester interface device (38).

With respect to claim 20, Slupsky ('202) discloses that a transmitter (18) (see Col. 2, line 31 " transmitter 18") configured to transmit test signals on at least one of said conductive structures (wireless I/O cells 14).

With respect to claim 21, Slupsky ('202) discloses each of said dies (12) comprises such a transmitter (18) (see Fig. 1).

With respect to claim 22, Slupsky ('202) discloses that a receiver (34) (see Col. 2, line 33 " receiver 34") configured to receive a test signals on at least one of said conductive structures (wireless I/O cells 14).

With respect to claim 23, Slupsky ('202) discloses each of said dies (12) comprises such a receiver (34) (see Fig. 1).

With respect to claim 24, Slupsky ('202) discloses that a transceiver (18, 34) (see Col. 1, "a transceiver 18"), configured to transmit test signals on at least one of said conductive structure(wireless I/O cells 14) and to receive a test signal induced on at least one of said conductive structures(wireless I/O cells 14).

With respect to claim 25, Slupsky ('202) discloses that each of said dies (12) comprises such a transceiver (see Fig. 1).

With respect to claim 26, Slupsky ('202) discloses a built in self test circuitry (see Col. 3, " using BIST (Built-In Self Test) techniques").

With respect to claim 28, Slupsky ('202) discloses means (38) for sending a test signal to a test channel without physically contacting said tester channel.

With respect to claim 29, Slupsky ('202) discloses that the means (wireless I/O cells 28) for receiving receives a plurality of test signals from a plurality of tester channels without physically contacting said plurality of tester channels (see Fig. 2)

With respect to claim 30, Slupsky ('202) discloses a means (computer 36) for controlling communications with a plurality of said tester channels (see Col. 2, lines 55-56).

With respect to the claims 46-49, Rostoker ('163)'s the overlying grid of lines can shield at least one of the dies from the electrical interference and can be sized to substantially cover at least one the dies (see Col. 6, lines 6-8).

3. Claims 39 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slupsky ('202) in view of Rostoker ('163) as applied to claims 16 and 27 above, and further in view of Reif et al (US Patent No. 7,067,909).

Slupsky ('202) in view of Rostoker ('163) fail to disclose a plurality of electrically conductor planes and insulating material disposed between the planes.

Reif et al ('909) disclose a multi-layer integrated semiconductor (see Fig. 1) comprising a plurality of electrically conductor planes (a first device layer 20 and a second device layer 40). Also Reif et al ('909) exclusively disclose insulating material (34,44) disposed between the planes (a first device layer 20 and a second device layer 40) (see Col. 3, lines 45-53).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the teaching of Reif et al ('909) into Slupsky ('202) in view of Rostoker ('163)'s apparatus because Reif et al ('909) disclose that isolation structure would substantially reduce the interference generated by the digital layer and its effect on the sensitive analog circuits (see Col. 2, lines 34-37).

Allowable Subject Matter

4. Claims 36- 38, 40-43 and 45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 36 and 41 are indicated allowable because the prior art in the record does not teach or suggest each die further comprises communication control circuitry (see Fig. 21 and Fig. 5, controller 702) and a test signal receiving means (see Fig. 5, transceiver 710) connected to the communication control circuitry (702). Claims 37-38 and 42-43 are dependent on claims 36 and 41 respectively and are indicated allowable accordingly. Claims 40 and 45 are indicated allowable because the prior art in the record does not teach or suggest a semiconductor wafer further comprising a power distribution plane 70 and a ground plane 72 as shown by Fig. 2.

Response to Arguments

5. Applicant's arguments filed 5/8/07 have been fully considered but they are not persuasive.

In the Remarks, applicant argued that the reference Slupsky ('202) does not teach the amended feature that the wafer comprises an electrically conductive shielding plane. Now this feature was taught by Rostoker ('163) (see rejection with respect to the claims 16 and 27 above).

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kwark (US Patent No. 7,215,133) discloses a contactless circuit testing dies on wafer (see Fig. 1-2).

Moore (US Patent No. 6,759,863) discloses a wireless testing of integrated circuits on wafers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y. Chan whose telephone number is 571-272-1956. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha T Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC
7/24/07

HA TRAN NGUYEN
SUPERVISORY PATENT EXAMINER